

EXHIBIT 019

U.S. Patent No. 7,366,818 (Radulescu & Goossens)

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Samsung Exynos 1280 System on Chip ¹
1. Integrated circuit comprising a plurality of processing modules (M, S) said modules being disposed on the same chip, and	Without conceding that the preamble of claim 1 of the '818 Patent is limiting, Samsung Electronics Co., Ltd.'s (hereinafter, "Samsung") Exynos 1280 system on chip (hereinafter, the "Exynos SoC") is an integrated circuit.

¹ The Exynos SoC is charted as a representative product made used, sold, offered for sale, and/or imported by or on behalf of Samsung. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein

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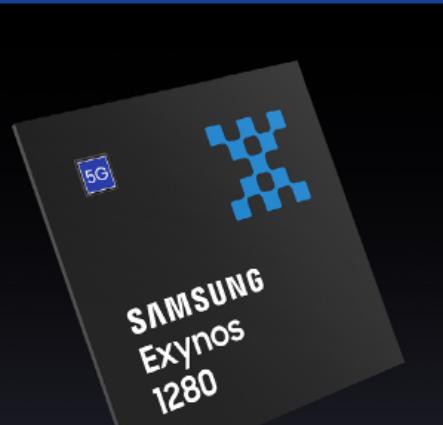
Product brief

Create infinite possibilities

Exynos 1280

Highlights

A mobile processor ready for 5G and AI
Advanced ISP and MFC for rich multimedia experience
Powerful octa-core CPU and GPU



5G for all

Exynos 1280 is a mobile processor based on a 64-bit RISC processor. It contains a 5G modem, which is compliant with two types of 5G network (Sub-6GHz and mmWave), as well as all legacy networks. It is built using an advanced 5nm EUV process for high power efficiency.

All-in-one processor for 5G

The Exynos 1280 embedded modem supports both sub-6GHz (Frequency Range

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	<p>https://semiconductor.samsung.com/resources/brochure/Exynos1280.pdf</p> <p>The Exynos SoC comprises a plurality of processing modules, for example Arm Cortex-A78 core, Cortex-A55 core, Arm Mali-G68 GPU, and AI Engine with NPU:</p> <h2 data-bbox="513 478 882 535">Specifications</h2> <table border="1" data-bbox="513 600 1883 1204"> <thead> <tr> <th colspan="2" data-bbox="977 600 1883 649">Exynos 1280</th></tr> </thead> <tbody> <tr> <td data-bbox="513 649 977 682">CPU</td><td data-bbox="977 649 1883 682">Cortex®-A78 x 2 + Cortex®-A55 x 6</td></tr> <tr> <td data-bbox="513 690 977 722">GPU</td><td data-bbox="977 690 1883 722">Mali™-G68</td></tr> <tr> <td data-bbox="513 731 977 763">AI</td><td data-bbox="977 731 1883 763">AI Engine with NPU</td></tr> <tr> <td data-bbox="513 771 977 845">Modem</td><td data-bbox="977 771 1883 845">5G NR Sub-6GHz 2.55Gbps (DL) / 1.28Gbps (UL) 5G NR mmWave 1.84Gbps (DL) / 0.92Gbps (UL) LTE Cat.18 6CC 1.2Gbps (DL) / Cat.18 2CC 200Mbps (UL)</td></tr> <tr> <td data-bbox="513 853 977 918">Connectivity</td><td data-bbox="977 853 1883 918">WiFi 802.11ac MIMO with Dual-band (2.4/5G), Bluetooth® 5.2, FM Radio Rx</td></tr> <tr> <td data-bbox="513 926 977 959">GNSS</td><td data-bbox="977 926 1883 959">Quad-constellation multi-signal for L1 and L5 GNSS</td></tr> <tr> <td data-bbox="513 967 977 1000">Camera</td><td data-bbox="977 967 1883 1000">Up to 108MP in single camera mode, Single-camera 32MP @30fps</td></tr> <tr> <td data-bbox="513 1008 977 1041">Video</td><td data-bbox="977 1008 1883 1041">4K 30fps encoding and decoding</td></tr> <tr> <td data-bbox="513 1049 977 1082">Display</td><td data-bbox="977 1049 1883 1082">Full HD+@120Hz</td></tr> <tr> <td data-bbox="513 1090 977 1122">Memory</td><td data-bbox="977 1090 1883 1122">LPDDR4x</td></tr> <tr> <td data-bbox="513 1130 977 1163">Storage</td><td data-bbox="977 1130 1883 1163">UFS v2.2</td></tr> <tr> <td data-bbox="513 1171 977 1204">Process</td><td data-bbox="977 1171 1883 1204">5nm</td></tr> </tbody> </table> <p>https://semiconductor.samsung.com/resources/brochure/Exynos1280.pdf</p>	Exynos 1280		CPU	Cortex®-A78 x 2 + Cortex®-A55 x 6	GPU	Mali™-G68	AI	AI Engine with NPU	Modem	5G NR Sub-6GHz 2.55Gbps (DL) / 1.28Gbps (UL) 5G NR mmWave 1.84Gbps (DL) / 0.92Gbps (UL) LTE Cat.18 6CC 1.2Gbps (DL) / Cat.18 2CC 200Mbps (UL)	Connectivity	WiFi 802.11ac MIMO with Dual-band (2.4/5G), Bluetooth® 5.2, FM Radio Rx	GNSS	Quad-constellation multi-signal for L1 and L5 GNSS	Camera	Up to 108MP in single camera mode, Single-camera 32MP @30fps	Video	4K 30fps encoding and decoding	Display	Full HD+@120Hz	Memory	LPDDR4x	Storage	UFS v2.2	Process	5nm
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a network (N; RN) arranged for providing at least	Without conceding that the preamble of claim 1 of the '818 Patent is limiting, the Exynos SoC utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the “Arteris NoC”) as a network (N; RN) arranged for providing connections																										

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<p>one connection between a first and at least one second module (M, S), wherein said modules communicate via a network on chip, and</p>	<p>between a first and at least one second module (M, S) in the Exynos SoC, wherein said modules communicate via a network on chip, either literally or under the doctrine of equivalents.</p> <p>The Exynos SoC utilizes utilizing the Arteris NoC as a data communication network:</p> <div data-bbox="508 442 1248 1367">  <p>Samsung uses Arteris FlexNoC IP in its Samsung Exynos mobile phone applications processors, digital baseband modems, 4K SUHD TVs and Artik IoT modules.</p> <p><a data-bbox="762 1225 988 1250" href="#">LEARN MORE »</p> </div> <p>https://web.archive.org/web/20210514110614/https://www.arteris.com/customers</p>

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	<p>Arteris IP FlexNoC® Interconnect Licensed by Samsung's System LSI Business for Digital TV Chips</p> <p>by Kurt Shuler, on April 23, 2019</p> <p>CAMPBELL, Calif. –April 23, 2019– Arteris IP, the world's leading supplier of innovative, silicon-proven network-on-chip (NoC) interconnect semiconductor intellectual property, today announced that Samsung's System LSI Business has renewed multiple Arteris IP FlexNoC Interconnect licenses for use in multiple high-performance digital TV (DTV) processing chips utilizing Samsung's latest semiconductor technology process nodes.</p> <p>“Over many years, FlexNoC interconnect IP has helped us accelerate implementation of our digital TV chip designs on our latest semiconductor process nodes. This core interconnect technology is required to develop complex and highly optimized chips in a predictable, low-risk fashion.”</p> <p>SAMSUNG</p> <p><i>Jaeyoul Lee, Vice President, Samsung Electronics</i></p> <p>Samsung first licensed FlexNoC interconnect IP in 2010. Since then, Samsung has used Arteris interconnect IP to enable complex SoC architectures in chips like the Exynos mobile processors and other electronic systems.</p> <p>https://www.arteris.com/press-releases/samsung-lsi-dtv-arteris-ip-flexnoc</p>

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	<p style="text-align: center;">Arteris Interconnect IP Solution Selected by Samsung for Mobile SoC Deployment</p> <p style="text-align: center;">by Kurt Shuler, on November 02, 2010</p> <p>Network-on-Chip (NoC) interconnect technology leader enables higher performance and more cost effective designs for mobile phone systems-on-chip (SoCs)</p> <p>SUNNYVALE, California — November 2, 2010 — Arteris, Inc., a leading supplier of on-chip interconnect IP solutions, today announced that Samsung Electronics Co., Ltd., has selected Arteris' interconnect solutions for multiple chips within Samsung's mobile SOC products. Samsung chose Arteris interconnect IP to support the high speed inter-chip communication requirements in next generation mobile SOC products.</p> <p>“<i>The Arteris interconnect IP offers us a convenient solution to handle the high speed communication needed between our SoC and external modem IC. Our customers will benefit from the lower BOM cost and power consumption as a result of this IP. We look forward to Arteris' interconnect IP helping us shorten development schedules and lower risks associated with compatibility.</i></p> <p style="text-align: right;"> Thomas Kim, Vice President, SoC Platform Development, System LSI, Samsung Electronics</p> <p>https://www.arteris.com/press-releases/pr_2010_nov_02?hsLang=en-us</p>

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	<p>In the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

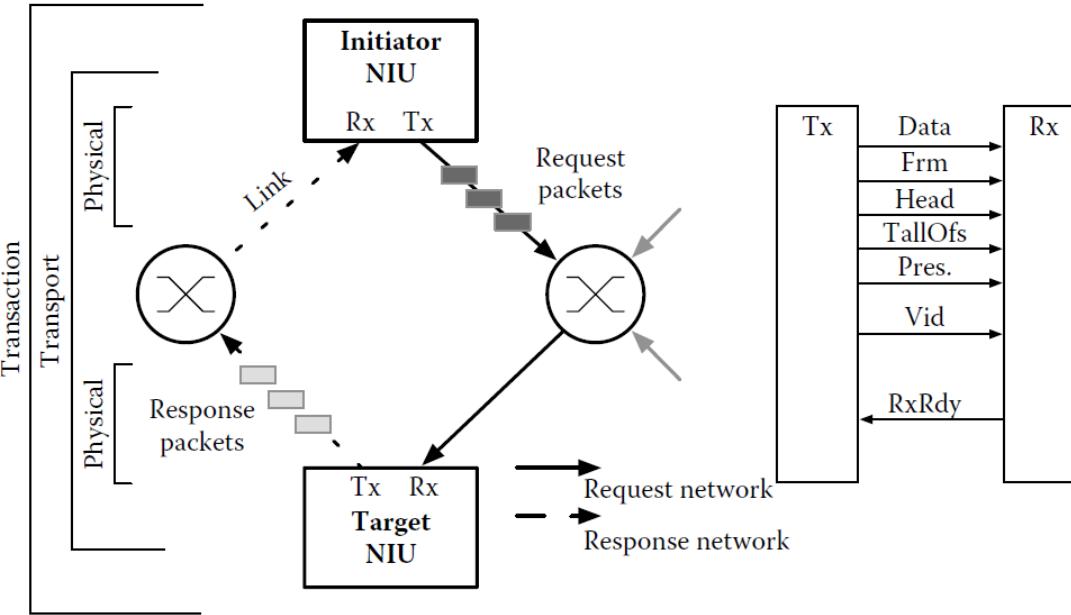
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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

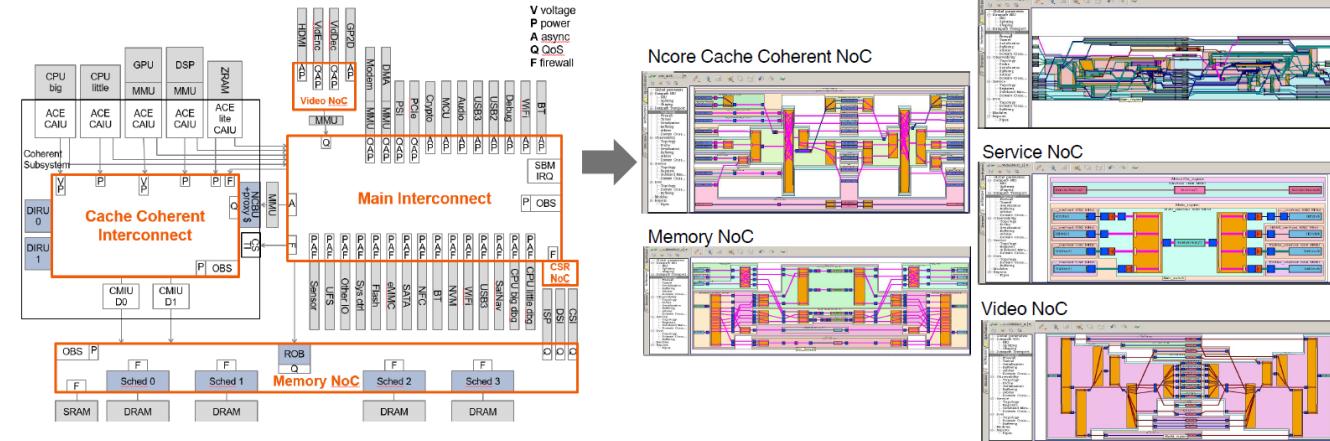
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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313; see <i>id</i> at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: "In this chapter we will present an MPSoC platform [...] using Arteris NoC as communication infrastructure.").</p> <p>A large SoC, such as the Exynos SoC may include multiple classes of Arteris NoC:</p>

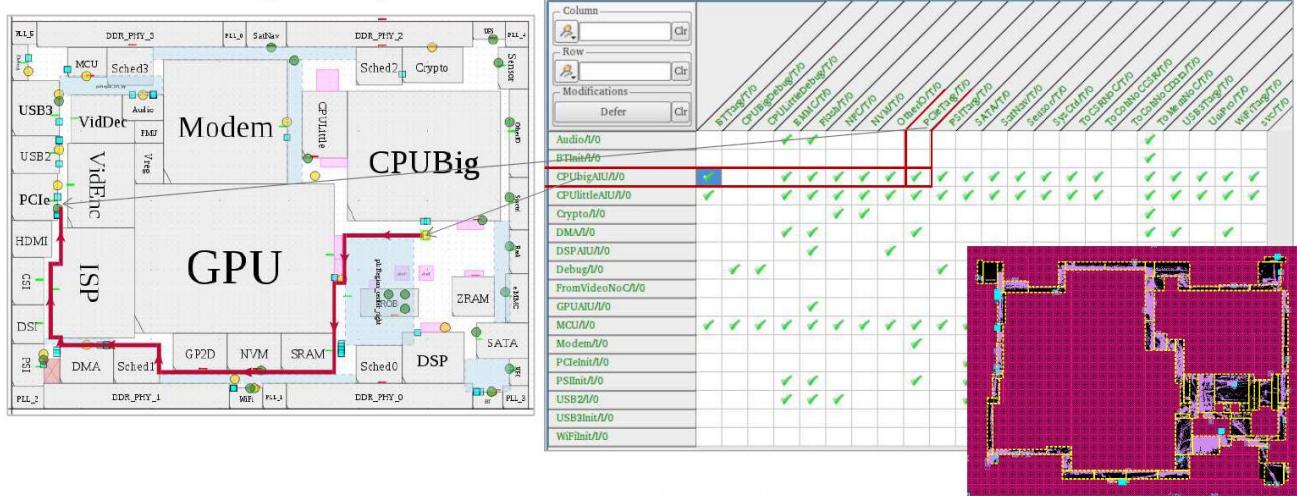
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<h2 data-bbox="530 298 1586 360">Logical Interconnect Topology Development</h2> <p data-bbox="530 368 1410 393">FLEXNOC & NCORE INTERCONNECT IPS DEFINE ARCHITECTURES</p>  <ul data-bbox="530 858 1755 959" style="list-style-type: none"> • ArChip16 Example: Large SoCs have multiple classes of interconnect <ul data-bbox="561 891 1241 915" style="list-style-type: none"> – Non-coherent, Coherent, Control/Status, Observability, etc. • Ncore & FlexNoC interconnects are managed separately from IP blocks, increasing design flexibility <p data-bbox="508 997 635 1021">ARTERIS IP</p> <p data-bbox="1106 997 1262 1021">ISPD 2018, 28 March 2018</p> <p data-bbox="1649 997 1818 1021">Copyright © 2018 Arteris IP 9</p> <p data-bbox="498 1086 1888 1160">See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.</p> <p data-bbox="498 1209 1888 1282">As a further illustration, connections between modules within the Arteris NoC may be defined by a connectivity table:</p>	

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	<p data-bbox="536 311 1833 368">Connectivity Map → Interconnect Connections → Layout</p>  <p data-bbox="536 864 1833 979"> <ul style="list-style-type: none"> Connectivity table defines interconnect connections within the floorplan Routes must pass through available channels in the floorplan Connectivity passes from initiator NIU to switch, to link, to RC buffers and finally to target NIU </p> <p data-bbox="536 1003 1833 1052"> ARTERIS IP ISPD 2018, 28 March 2018 Copyright © 2018 Arteris IP 12 </p> <p data-bbox="502 1068 1883 1142">See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.</p>
<p>wherein said connection supports transactions comprising outgoing messages</p>	<p>The Arteris NoC utilized by the Exynos SoC has a connection that supports transactions comprising outgoing messages from the first module to the second modules and return messages from the second modules to the first module, either literally or under the doctrine of equivalents.</p> <p>For example, in the Arteris NoC, "[m]ost transactions require the following two-step transfers," including "[a] master send[ing] request packets" and "the slave return[ing] response packets":</p>

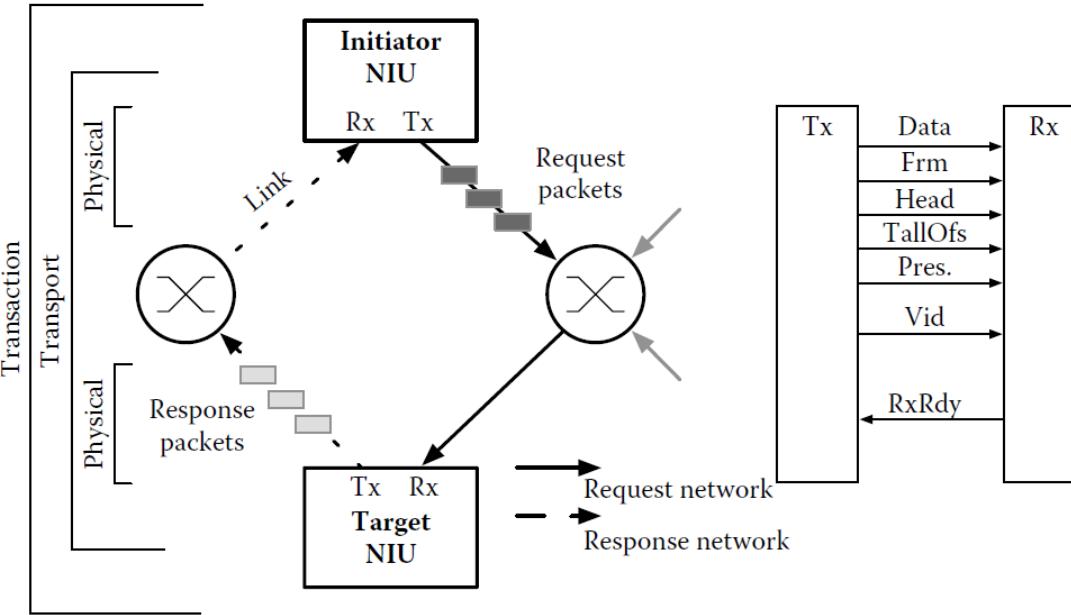
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from the first module to the second modules and return messages from the second modules to the first module	<p>11.3.1.1 <i>Transaction Layer</i></p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU’s Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	<p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p>
the integrated circuit comprising at least one dropping means (DM) for dropping data exchanged by	<p>The Arteris NoC utilized by the Exynos SoC has at least one dropping means (DM) for dropping data exchanged by said first and second module (M, S), either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC addresses packet corruption using, among other mechanisms, "packet validity checker" and "initiator timeout," which may result in data being dropped:</p>

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said first and second module (M, S), and	<p>Example NoC Functional Safety Mechanisms</p> <table border="1" data-bbox="544 425 1848 899"> <thead> <tr> <th data-bbox="544 425 903 470">Function</th><th data-bbox="903 425 1326 470">Failure Modes</th><th data-bbox="1326 425 1848 470">Safety Mechanisms</th></tr> </thead> <tbody> <tr> <td data-bbox="544 470 903 556">Packetization</td><td data-bbox="903 470 1326 556">External interface corruption; External protocol violation; Packet corruption</td><td data-bbox="1326 470 1848 556">External placeholder (ECC/Parity); Packet validity checker; Duplication; Initiator timeout</td></tr> <tr> <td data-bbox="544 556 903 643">Transport</td><td data-bbox="903 556 1326 643">Packet corruption</td><td data-bbox="1326 556 1848 643">ECC/Parity + checker; Packet validity checker; Initiator timeout</td></tr> <tr> <td data-bbox="544 643 903 780">Clocking and reset</td><td data-bbox="903 643 1326 780">Clock / reset glitch; Frequency error; Wrong clock gating</td><td data-bbox="1326 643 1848 780">External Timeout AoU; Initiator timeout; Packet validity checker; Percentage safe AoU</td></tr> <tr> <td data-bbox="544 780 903 833">Safety reporting</td><td data-bbox="903 780 1326 833">Missed / incorrect reporting; unexpected reporting of Fault</td><td data-bbox="1326 780 1848 833">Register parity; Regular check AoU</td></tr> <tr> <td data-bbox="544 833 903 899">Safety mechanism</td><td data-bbox="903 833 1326 899">Missed / incorrect reporting; unexpected reporting of Fault</td><td data-bbox="1326 833 1848 899">BIST; Regular check AoU</td></tr> </tbody> </table>  <p>10 © 2018 Arm Limited</p> <p>ARTERISIP + arm</p> <p>Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP, https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation, at 10.</p> <p>As a further example, the Arteris NoC includes “packet validity checking” and “transaction timeout” for error resiliency, which may result in data being dropped:</p>	Function	Failure Modes	Safety Mechanisms	Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; Initiator timeout	Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout	Clocking and reset	Clock / reset glitch; Frequency error; Wrong clock gating	External Timeout AoU; Initiator timeout; Packet validity checker; Percentage safe AoU	Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU	Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU			
Function	Failure Modes	Safety Mechanisms																				
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	<p><i>A. Advanced Data Protection and Reliability for SoC Interconnects</i></p> <p>Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller.</p> <p>The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent.</p> <p>Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf at 7.</p> <p>As a further example, in the Arteris NoC, “[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC,” which may result in data being dropped:</p>

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	<p><i>C. Transaction Timeout</i></p> <p>Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption.</p> <p>SoC Reliability Features in the FlexNoC Resilience Package, http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf at 2.</p>
at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN),	<p>The Arteris NoC utilized by the Exynos SoC has at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN), either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p>

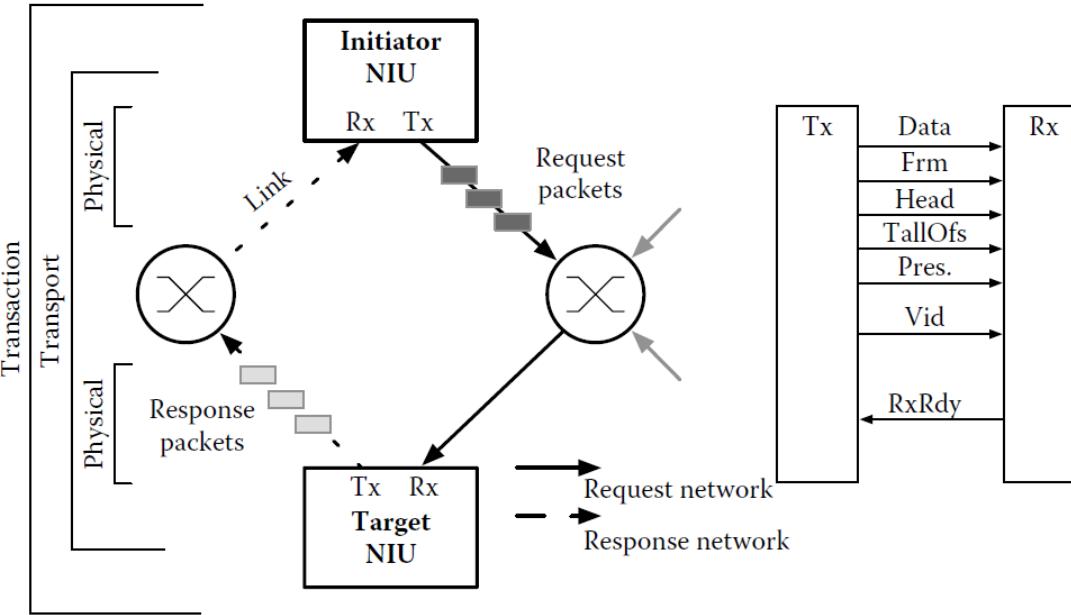
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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Initiator NIUs are “used to connect a master node to the NoC,” and the Target NIUs are “used to connect a slave node to the NoC”:</p>

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	<p>11.3.2 Network Interface Units</p> <p>The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p>In the Arteris NoC “Initiator NIU units...enable connection between an AMBA-AHB master IP and the NoC”:</p>

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	<p>11.3.2.1 <i>Initiator NIU Units</i></p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can</p>

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	<p>burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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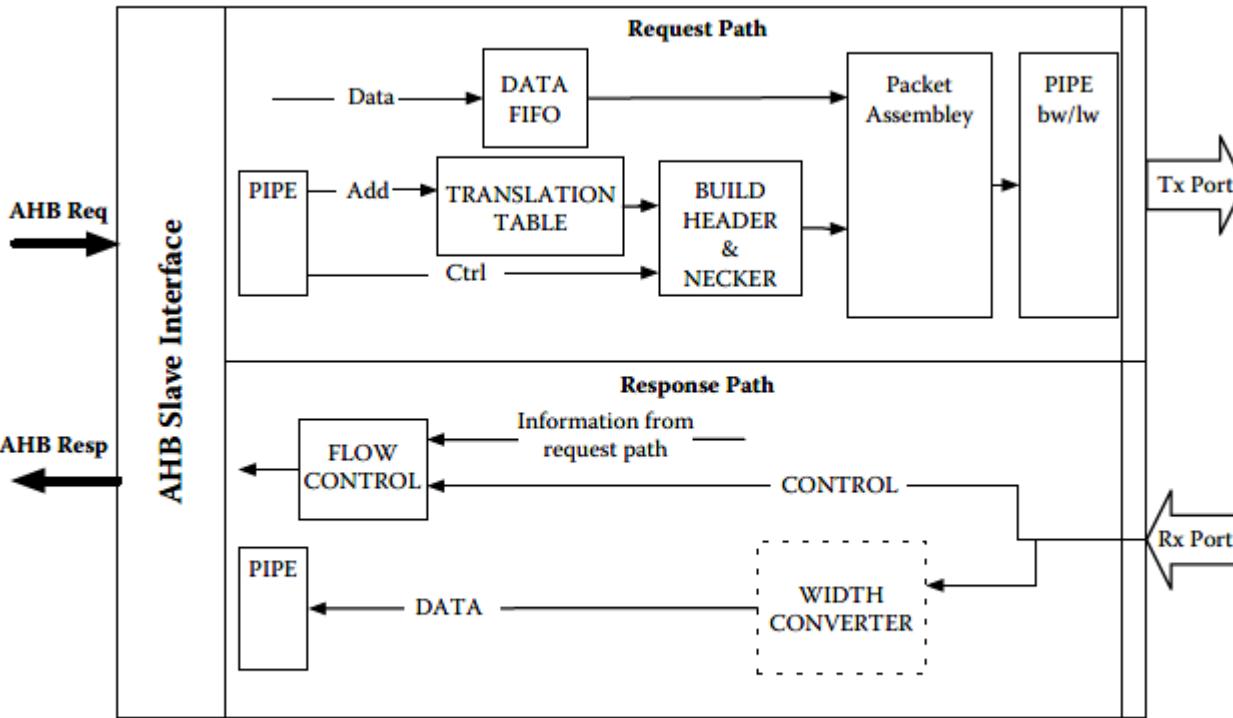
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	<p style="text-align: center;">NIU Architecture</p>  <p>Request Path</p> <p>Response Path</p> <p>AHB Req → AHB Slave Interface → PIPE → DATA FIFO → TRANSLATION TABLE → BUILD HEADER & NECKER → Packet Assembly → PIPE bw/lw → Tx Port</p> <p>AHB Resp ← FLOW CONTROL ← PIPE ← WIDTH CONVERTER ← DATA ← AHB Slave Interface</p> <p>Information from request path → FLOW CONTROL</p> <p>CONTROL → FLOW CONTROL</p> <p>CONTROL → WIDTH CONVERTER</p>

FIGURE 11.4

Network interface unit: Initiator architecture.

Networks-On-Chips Theory and Practice, <https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0>, at 317-318.

As further example, "Target NIU units enable connection of a slave IP to the NoC by translating

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	<p>NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets":</p> <p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always 32 bits wide, but the actual address space size may be downsized by setting a hardware parameter. Unused AHB address bits are then driven to zero. The NTTP request packet is then translated into one or more corresponding AHB accesses, depending on the transaction type (word aligned or nonaligned access). For example, if the request is an atomic Store, or a Load that can fit an AHB burst of specified length, then such a burst is generated. Otherwise, an AHB burst with unspecified length is generated.</p>

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<p>Target NIU Architecture</p> <p>Request Path</p> <p>Response Path</p> <p>A vertical AHB Master Interface connects the Request Path and Response Path, with AHB Req and AHB Resp arrows.</p> <p>FIGURE 11.5 Network interface unit: Target architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 318-319.</p>	

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<p>wherein said interface means (ANIP, PNIP) comprises a first dropping means (DM) for dropping data, and</p>	<p>The interface means of the Arteris NoC utilized by the Exynos SoC comprises a first dropping means (DM) for dropping data, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which include Initiator NIUs, that are “used to connect a master node to the NoC,” and the Target NIUs, that are “used to connect a slave node to the NoC”:</p> <p>11.3.2 Network Interface Units</p> <p>The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p>For example, the Arteris NoC addresses packet corruption using, among other mechanisms, “packet validity checker” and “initiator timeout,” which may result in data being dropped:</p>

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Example NoC Functional Safety Mechanisms		
Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; Initiator timeout
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error; Wrong clock gating	External Timeout AoU; Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU
Functions → Failure Modes → Safety Mechanisms		
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ARTERIS IP + arm		
<p>Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP, https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation, at 10.</p> <p>As a further example, the Arteris NoC “can pass IP-generated error-correcting code (ECC) information through the NoC between the socket interfaces” and includes “packet validity checking” and “transaction timeout” for error resiliency, which may result in data being dropped:</p>		

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	<p><i>A. Advanced Data Protection and Reliability for SoC Interconnects</i></p> <p>Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller.</p> <p>The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent.</p> <p>Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf at 7.</p> <p>As a further example, in the Arteris NoC, "[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC," which may result in data being dropped:</p>

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	<p><i>C. Transaction Timeout</i></p> <p>Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption.</p> <p>SoC Reliability Features in the FlexNoC Resilience Package, http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf at 2.</p>
wherein the dropping of data and therefore the transaction completion can be controlled by the interface means.	<p>In the Arteris NoC utilized by the Exynos SoC, the transaction completion can be controlled by the interface means, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which include Initiator NIUs, that are “used to connect a master node to the NoC,” and the Target NIUs, that are “used to connect a slave node to the NoC”:</p> <p>11.3.2 Network Interface Units</p> <p>The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p>

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<small>10 © 2018 Arm Limited</small>		
		
<p>Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP, https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation, at 10.</p> <p>As a further example, the Arteris NoC “can pass IP-generated error-correcting code (ECC) information through the NoC between the socket interfaces” and includes “packet validity checking” and “transaction timeout” for error resiliency, which may result in data being dropped:</p>		

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